CLAIMS

1. An apparatus for memory error control coding comprising:

a first circuit configured to generate a multi-bit digital syndrome signal in response to a read data signal and a read parity signal; and

a second circuit configured to (i) detect an error when said bits of said syndrome signal are not all the same state and (ii) generate an error location signal in response said syndrome signal, wherein said error location signal is generated in response to fewer than all of said bits of said syndrome signal.

2. The apparatus according to claim 1, wherein all of said bits of said syndrome signal are at a particular state when no error is detected in said read data and parity signals and said particular state comprises a digital 1.

3. The apparatus according to claim 1, wherein said apparatus is configured to present said read data and parity signals at an output when no error is detected in said read data and parity signals.

4. The apparatus according to claim 1, wherein said apparatus comprises a memory circuit configured to (i) receive a data input signal and a parity signal and (ii) present said read data and parity signals during a read operation.

5. The apparatus according to claim 1, wherein said second circuit is configured to generate (i) a single error signal when a single bit error is detected in said read data and parity signals, (ii) a double error signal when an error is detected in two bits of said read data and parity signals, and (iii) an error detected signal when either said single error signal or said double error signal are generated in response to said syndrome signal.

6. The apparatus according to claim 1, wherein said apparatus is configured to generate a corrected representation of said read data and parity signals when a single bit error is detected.

7. The apparatus according to claim 1, wherein said second circuit comprises an inverter at an input for each of said bits of said syndrome signal.

8. The apparatus according to claim 1, further comprising:

an encoder circuit configured to generate said parity signal in response to a data input signal, wherein said encoder circuit comprises a type selected from the group consisting of (i) non-inverting exclusive-OR gates, (ii) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (iii) inverting exclusive-OR gates, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) inverting exclusive-NOR gates, (vii) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

9. The apparatus according to claim 1, wherein said second circuit comprises:

one or more OR gates configured to receive said syndrome signal and present said error detected signal;

one or more exclusive-OR gates configured to receive said syndrome signal and present an intermediate signal;

one or more AND gates configured to present said single error signal in response to said error detected signal and said intermediate signal; and

an AND gate configured to present said double error signal in response to said error detected signal and an inverse of said intermediate signal.

10. The apparatus according to claim 9, wherein said single error signal comprises a multi-bit digital signal.

11. The apparatus according to claim 1, wherein said syndrome signal is generated using a type of syndrome signal encoder selected from the group consisting of (i) non-inverting exclusive-OR gates, (ii) non-inverting exclusive-OR gates with an output inverted by a NOT gate, (iii) inverting exclusive-OR gates, (iv) inverting exclusive-OR gates with an output inverted by a NOT gate, (v) non-inverting exclusive-NOR gates, (vi) non-inverting exclusive-NOR gates with an output inverted by a NOT gate, (vii) inverting exclusive-NOR gates, and (viii) inverting exclusive-NOR gates with an output inverted by a NOT gate.

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12. The apparatus according to claim 1, wherein said apparatus comprises one or more logic gates configured to receive said syndrome signal and a bypass signal, wherein (i) said syndrome signal is presented in response to said bypass signal having a first state and (ii) said error location generation is disabled in response to said bypass signal having a second state.

13. The apparatus according to claim 12, wherein said one or more logic gates are selected from the group consisting of gates AND, NAND, NOR, and OR gates.

14. An apparatus for memory error control coding comprising:

means for generating a multi-bit digital syndrome signal in response to a read data signal and a read parity signal; and

means for (i) detecting an error when said bits of said syndrome signal are not all the same state and (ii) generating an error location signal in response said syndrome signal, wherein said error location signal is generated in response to fewer than all of said bits of said syndrome signal.

15. A method for memory error coding correcting comprising the steps of:

(A) generating a multi-bit digital syndrome signal in response to a read data signal and a read parity signal; and

(B) detecting an error when said bits of said syndrome signal are not all the same state and generating an error location signal in response to said syndrome signal, wherein said error location signal is generated in response to fewer than all of said bits of said syndrome signal.

16. The method according to claim 15, wherein all of said bits of said syndrome signal are at a particular state when no error is detected in said read data and parity signals and said particular state comprises a digital 1.

17. The apparatus according to claim 15, wherein step (B) further comprises the step of:

bypassing said error location signal generating sub-step in response to a control signal.

Sub a3

18. The apparatus according to claim 15, wherein step (B) further comprises the sub-steps of:

generating a single error signal when a single bit error is detected in said read data signal or parity signals;

generating a double error signal when an error is detected in two bits of said read data or parity signals; and

generating an error detected signal when either said single error signal or said double error signal are generated in response to said syndrome signal.

19. The method according to claim 15, wherein said method further comprises the step of:

presenting said read data and parity signals when no error is detected in said read data and parity signals.

20. The method according to claim 15, wherein said method further comprises the step of:

generating a corrected representation of said read data and parity signals when said single bit error is detected.

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